

# Design of Inductors in Organic Substrates For 1-3 GHz Wireless Applications

Sidharth Dalmia\*, Farrokh Ayazi, Madhavan Swaminathan\*\*, Sung Hwan Min, Seock Hee Lee, Woopoung Kim, Dongsu Kim, Swapan Bhattacharya, Venky Sundaram, George White, and Rao Tummala

School of Electrical and Computer Engineering  
Georgia Institute of Technology  
Atlanta, GA 30332-0250

Email: \*dalmia@ee.gatech.edu, \*\*madhavan.swaminathan@ee.gatech.edu, \*\*Phone: 404-894-3340

**Abstract** — High Q inductors with maximum quality factors in the range of 180-60 have been obtained at frequencies in the 1-3 GHz band for inductances in the range of 1nH to 20nH using a low-temperature organic laminate build-up process. This is the first time such high Q inductors have been demonstrated in this technology. The different inductor designs, optimization schemes, and trade-offs between different topologies, have been discussed in this paper.

It is appropriate that the discussion for inductors begin with microstrip loop inductors since this particular topology has already been introduced in [1]. This discussion will be followed by the microstrip spiral in section III, and the CPW loop topology in section IV and finally a comparison will be made based on a few key parameters such as size, spacing to ground, circular vs. rectangular configurations, and ease of modeling.

## I. INTRODUCTION

This paper presents results for inductors fabricated a low-cost low-temperature large area organic process. This is an alternative to high temperature processes such as LTCC and MCM-D. In [1] results were presented for microstrip loop inductors with inductances in the range of 1nH-12nH and Q in the range of 30-100 using the low-temperature organic process. The inductor topologies have been modified in this paper to amplify the positive mutual inductance between the loops to increase the inductance. In addition, spiral inductors with wide metal width have been fabricated with inductances and Qs similar to the microstrip loop inductors. By modifying the topology of the microstrip loops into a co-planar waveguide with hollow-ground, the Q of the inductors were increased by 20-30%. This paper presents the various inductor designs specific to the organic process with details on the optimization schemes used and the trade-offs between the different topologies.

The testbed discussed in this paper was processed using just one build up layer of Dupont Vialux. This was done to ensure maximum possible yield by eliminating via registration and alignment problems encountered during the fabrication. The cross-section of the current test vehicle is shown in Figure 1. Some of the key design rules that were set forth are explained in Figure 1. No plated through holes (PTH) were used for backside connections. Figure 2 is one of the quadrants of the 12" \* 12" testbed. A number of inductors with varying topologies were designed for optimal performance in the 1, 1.8, and 2.4 GHz bands of interest.

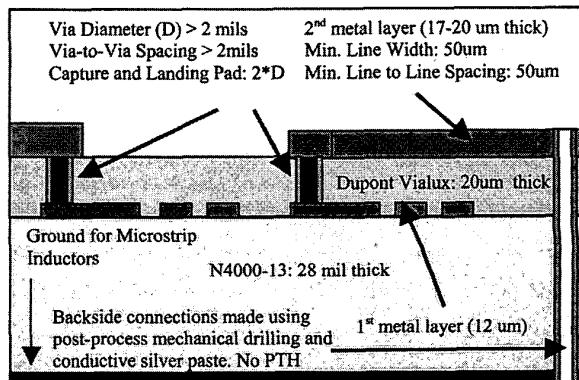


Figure 1. Cross-section of Testbed  
4 inch

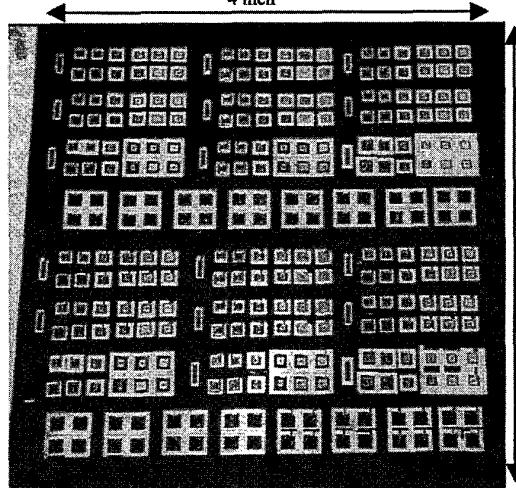


Figure 2. Top View of 4" \* 4" quadrant of testbed  
(Fabricated at PRC, May 2001)

## II. MICROSTRIP LOOP INDUCTORS

Figure 3 shows the top view of several microstrip loop inductors with a common ground (indicated in Figure 1), which is ~29 mils (28 mils of N4000-13 and 1 mil of Vialux) below the signal lines. A maximum of  $4.5\text{mm}^2$  area was allotted for each inductor. Prior to this, a maximum Q of 99 was obtained for a 11nH microstrip loop inductor at 2.2 GHz and a SRF of 3.6 GHz[1]. However, the ground to signal separation was approximately 38~40 mils.

Table 1 shows the measured data for the loop inductors in Figure 3. The data was collected using Agilent's 8720ES Vector Network Analyzer (VNA). The data was collected using a 500um pitch Cascade Microtech GSG probe after using a 1-port Short-Open-Load calibration with an averaging factor of 32 and 1601 points for bandwidths of 2 GHz. As seen inductors 1, 4 and 5 are well suited for applications around 2 GHz and inductors 2 and 3 are well suited for applications around 1 GHz. It should be noted that the separation of 29 mils between the signal lines and ground should be also be considered as a part of the inductor size and area. However, since most comparison are based on the top surface or 2D area, only the surface area is shown in Table 1. For the sake of

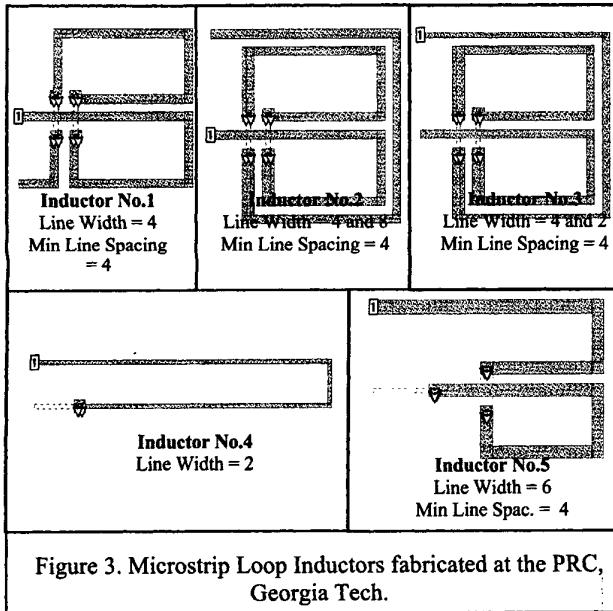


Figure 3. Microstrip Loop Inductors fabricated at the PRC, Georgia Tech.

comparison and validity, Inductor 5 was modeled using the multiple coupled line data from ANSOFT2D and the techniques in [3]. No scalable models for bends and vias were developed in the interest of time and were treated as shorts. The comparison between the measured data and

modeled data can be seen in Figures 4 and 5. As seen, there is good agreement between the two sets of data and speaks again for the validity of the measurement and modeling technique.

Even with a lesser separation between the ground and signal lines, it is seen that the designs for loop inductors can be easily optimized for sufficiently high Q factors at high frequencies keeping the area constrained to a certain maximum.

Table 1. Measured data for Microstrip Loop Inductors shown in Figure 3.

Inductor	Max Q (Peak Q Frequency)	Effective Inductance (nH)	Area mm <sup>2</sup>	SRF GHz
Inductor 1	Q=85 at 2.2 GHz	L=10.2	3.5	5
Inductor 2	Q=80 at 1 GHz	L=15	4	3.2
Inductor 3	Q=70 at 1 GHz	L=17	4	3
Inductor 4	Q=90 at 2.4	L=7.68	3.5	7.2
Inductor 5	Q=110 at 2.1	L=7.5	4.3	6

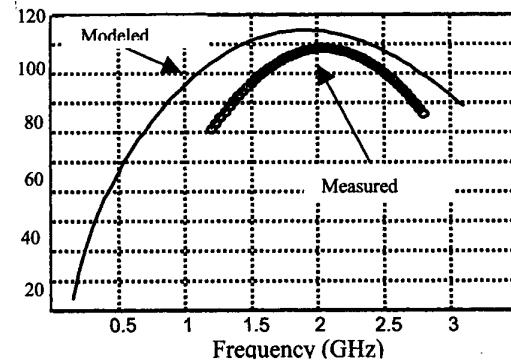


Figure 4. Q vs. Freq for Microstrip Loop Inductor #5

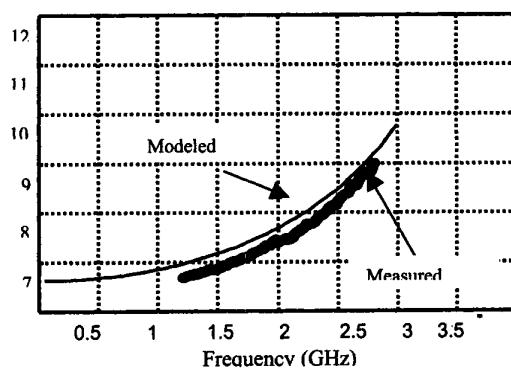


Figure 5. Inductance (nH) vs. Freq for Microstrip Loop Inductor #5

### III. MICROSTRIP SPIRAL INDUCTORS

Another microstrip type design that was investigated was wide-strip (4mils-40mils) narrow-spacing (2mils-4mils) spiral inductors. As stated earlier narrow-strip narrow-spacing spirals provide high inductances but exhibit low Q factors because of the associated skin-effect losses, eddy current losses and proximity effect losses. With a ground-to-signal spacing of 29 mils, the associated inductances that can be obtained from multi-turn narrow-strip narrow-spacing inductors is far too much than what is required for 2 GHz frequency applications. Wide-strip narrow-spacing spirals lower the associated inductance and suffer from eddy current and proximity effects; however, the wide strips and the associated metal thickness (17-20um) together help reduce the skin-effect and DC resistance significantly. Keeping the spacing narrow (2-4mils) helps keep the size of the inductors small and also helps increase the positive mutual inductance between lines. The capacitance to ground does increase due to the increase widths, reducing the effective inductances and lowering the SRF. Nonetheless, through a simple optimization routine ideally suited for multi-turn spirals, sufficient inductances (1nH-10nH) with maximum Q factors at 1 GHz and 2 GHz and SRF > 5 GHz. The optimization technique and results for wide-strip narrow-spacing spirals is mentioned ahead. Figure 6 shows the top view of five different spiral inductors with line widths varying from 7 mils to 34 mils but the spacing kept at a maximum of 4 mils. This ensures every inductor less than  $4.5\text{mm}^2$  and suitable for integration with other components. Figure 7 shows the measured Q factors for Inductor #7, #9 and #10 of Figure 30. Table 2 shows the measured data for the spiral inductors. The inductors were again measured using the same setup used to measure the loop inductors.

As seen in Table 1 and Table 2, same-sized narrow-space, wide-strip spirals and loop inductors exhibit the same properties in terms of the achievable Q factors and achievable nominal inductances at desired frequencies. However, the distinct advantage when using loop inductors is that hybrid techniques such as the coupled line approach [3] can help predict the frequency responses more accurately than empirical equations that are conventionally used for spiral inductors. The best-suited technique for tightly wound spirals such as the ones discussed here would be to use relatively fast engines such as SONNET [4]; SONNET predicts the effective inductance and SRF accurately but overestimates the associated loss in most instances. The technique mentioned in [5], well-suited for microstrip spirals on silicon substrates, can be modified for modeling inductors on organic substrates, but the accuracy is limited to 1-turn and 2-turn inductors. This is probably

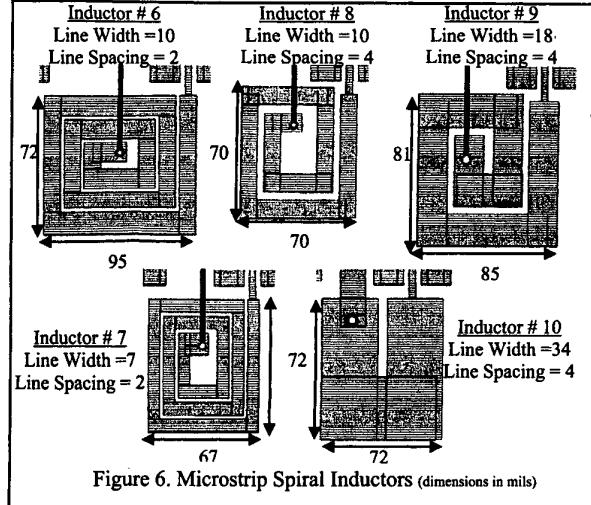


Figure 6. Microstrip Spiral Inductors (dimensions in mils)

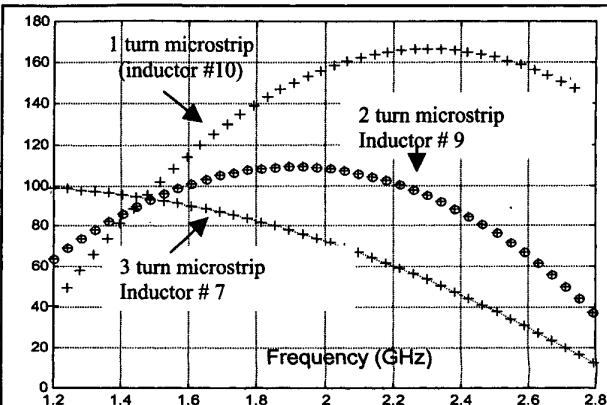


Figure 7. Measured Qs for Inductor #7, #9, and #10 of Figure 6

Table 2. Measured data for Microstrip Spiral Inductors shown in Figure 6.

Inductor	Max Q (Peak Q Frequency)	Effective Inductance (nH)	Area $\text{mm}^2$	SRF (GHz)
Inductor 6	80 at 1.5 GHz	$L = 12$	4.4	3.9
Inductor 7	100 at 1.0 GHz	$L = 12$	3.1	3.2
Inductor 8	100 at 2.0 GHz	$L = 7$	3.2	6.8
Inductor 9	110 at 2.0 GHz	$L = 5.2$	4.5	7
Inductor 10	170 at 2.4 GHz	$L = 1.5$	3.2	8.5

because the equations include coupling of adjacent lines and not higher order coupling. For spirals with more 2 turns the designs can be optimized using SONNET.

Although, both the loop and spiral inductors provided sufficiently high Q factors for the required inductances, the designs do require a connection to the backside; in other words, without the luxury of several through holes, referencing other components to the same ground may become a hindrance during the design stage. Another

obvious disadvantage with the microstrip topology at higher frequencies is the current crowding on the ground plane right below the device.

#### IV. CPW / HOLLOW-GROUND INDUCTORS

Figure 8 shows the top view of several CPW loop inductors that were also implemented. Unlike the microstrip inductors, the ground or the reference for the devices are the wide ground rings around the devices themselves as shown in Figure 8. Although this eliminates the need for backside connections, it does increase the area of the device. For this reason a CPW or hollow-ground topology was also investigated. The CPW topology ensures the proximity of the ground since the structure and ground are co-planar and also prevents the current crowding on the ground planes by forcing the currents to flow around the device on the larger area coplanar ground. Table 3 shows measured CPW inductors results using the same procedure outlined for the spiral and loop inductors. The same modeling technique used to model the microstrip loop inductors was used to model the CPW loop inductors. The modeling technique again shows good agreement with the measured data.

#### V. COMPARISONS AND CONCLUSION

The work presented in this paper shows an attractive alternative to high-temperature processes such as LTCC [6] and MCM-D [7] for high Q embedded passive applications. Aggressive feature sizes of 2 mil lines with 2 mil spacing and 2 mil microvias help keep the size of devices small. The microstrip loop and spiral inductors with sizes  $< 4.5\text{mm}^2$  are ideally suited for integration in compact microwave circuits. The CPW inductors, though larger in size, offer the advantage of higher Q factors and access to ground reference on the same layer. A point worth mentioning is that the thickness of the core  $\sim 28$  mils, is an extremely important requirement for the optimized performance of all devices. This ensures a large separation of the ground and signal lines, which in turn helps increase the inductance, reduce the resistive loss and reduce the parasitic capacitance. In both LTCC and MCM-D such thick cores can only be built by stacking up several layers, thereby increasing the process steps. In organic technology the core that is used to build up layers on, is inherently 28-40 mils and ideal for embedded inductor applications. One build up layer, with microvias, provides the necessary means for under-routings and connectivity between devices. Finally, the authors would like to thank Dr. Steve Kenney and his group at Georgia Tech for their help in making measurements.

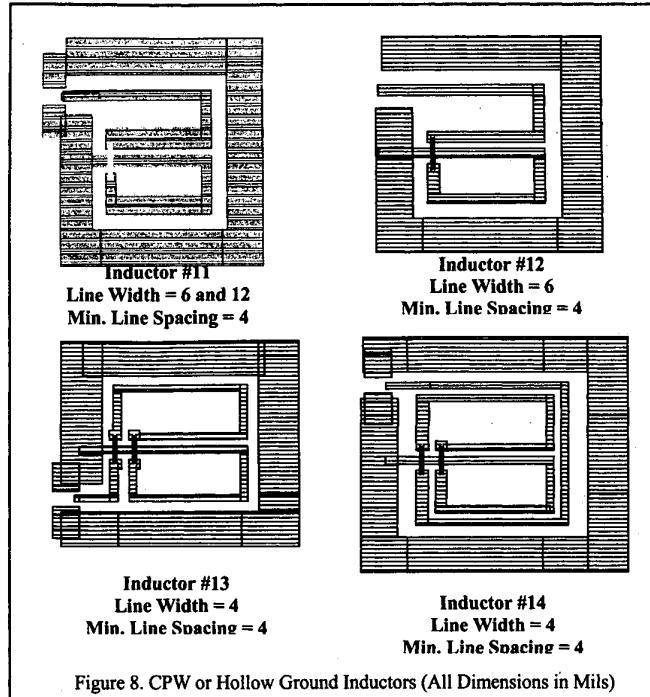


Figure 8. CPW or Hollow Ground Inductors (All Dimensions in Mils)

Table 3. Measured data for CPW Loop Inductors shown in Figure 8.

Inductor	Max Q (at Freq [GHz])	Effective Inductance (nH)	Area mm <sup>2</sup>	SRF GHz
Inductor 11	Q=180 at 2.2	L = 4.8	9	5.5
Inductor 12	Q=140 at 1.9	L = 5.8	9	5.2
Inductor 13	Q=120 at 1.8	L = 8.8	9.5	5
Inductor 14	Q=70 at 1.8	L = 14	9.5	5

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